

CoNNeCT's Approach for the Development of Three Software Defined Radios for Space Application

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Abstract— National Aeronautics and Space Administration (NASA) is developing an on-orbit, adaptable, Software Defined Radios (SDR)/Space Telecommunications Radio System (STRS)-based testbed facility to conduct a suite of experiments to advance technologies, reduce risk, and enable future mission capabilities. The flight system, referred to as the “SCAN Testbed” will be launched on an HTV-3 no earlier than May of 2012 and will operate on an external pallet on the truss of the International Space Station (ISS) for up to five years. The Communications, Navigation, and Networking reConfigurable Testbed (CoNNeCT) Project, developing the SCAN Testbed, will provide NASA, industry, other Government agencies, and academic partners the opportunity to develop and field communications, navigation, and networking applications in the laboratory and space environment based on reconfigurable, software defined radio platforms and the Space Telecommunications Radio System (STRS) Architecture.

Three flight qualified SDRs platforms were developed, each with verified waveforms that are compatible with NASA's Tracking and Data Relay Satellite System (TDRSS). The waveforms and the Operating Environment are compliant with NASA's software defined radio standard architecture, STRS. Each of the three flight model (FM) SDRs has a corresponding breadboard and engineering model (EM) with lower fidelity than the corresponding flight unit.

Procuring, developing, and testing SDRs differs from the traditional hardware-based radio approach. Methods to develop hardware platforms need to be tailored to accommodate a “software” application that provides functions traditionally performed in hardware. To accommodate upgrades, the platform must be specified with assumptions for broader application but still be testable and not exceed Size, Weight, and Power (SWaP) expectations. Ideally, the applications (waveforms) operating on the platform should be specified separately to accommodate portability to other platforms and support multiple entities developing the platform from the application. To support future flight upgrades to the flight SDRs, development and verification platforms are necessary in addition to the flight system.

This paper provides details on the approach used to procure and develop the SDR systems for CoNNeCT and provide suggestions for similar developments. Unique development approaches for each SDR were used which provides a rare opportunity to compare approaches and provide recommendations for future space missions considering the use of an SDR. Three case studies were examined. In two cases, the SDR vendor (General Dynamics and Harris) was the

integrated platform and waveform provider. In these cases, the platform and waveform requirements were considered together by the vendor using high level analysis to support the division of the requirements. In the Harris SDR case, the platform and waveform specification was then integrated into a single document. This case study was for a first generation platform, which offers significant processing and reconfigurability, but is not optimized for SWaP. This provides a test bed platform for many investigations of future capabilities, but requires additional SWaP than optimized flight radios. In the GD case, the specifications were provided separately. The GD SDR leverages existing platforms with minor changes to the Radio Frequency (RF) portions. The most significant change to the CoNNeCT GD SDR from previous platforms was the addition of a reconfigurable processor. The capability tests the next generation SDR, but offers limited capacity and reconfigurability. In the case of the JPL SDR, the platform was developed by JPL and Cincinnati Electronics. Goddard Space Flight Center (GSFC) provided a waveform that was developed on a ground-based development platform, and Glenn Research Center (GRC) ported the waveform to the flight platform and performed the integrated test and acceptance of the subsystem. This last case also leverages an existing platform development, and offers more capacity for reconfigurability than the second case.

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1. INTRODUCTION

As part of the development and testing of the three SDRs for the CoNNeCT system, knowledge was gained on improving the approach for writing requirements, developing the hardware platform, OE, and waveforms, and testing the individual subsystems and the integrated system. This paper captures, at a high level, some of this knowledge for future SDR platform and waveform developers.

This paper is comprised of a brief overview of the CoNeCT system and a description and figure of each SDR in Section 2. Sections 3-5 describe the procurement, requirement, development, and test approach for each SDR. It also includes the lessons the authors have learned that may benefit future SDR development. Section 6 provides a summary of the paper and conclusions.

2. CoNeCT SYSTEM OVERVIEW

The SCAN Testbed consists of reconfigurable and reprogrammable software defined radio transceivers/transponders operating at S-band, Ka-band, and L-band, along with the required RF/antenna systems

necessary for communications. The SCAN Testbed will be resident on an EXPRESS Logistics Carrier (ELC) on an exterior truss of the International Space Station. The system is designed to operate for a minimum of two years

The flight system aboard ISS within the system architecture is shown in Figure 1. The three SDRs will provide S-band duplex Radio Frequency (RF) links directly with the ground, S and Ka-band duplex RF links with the Tracking and Data Relay Satellite System (TDRSS), and L-Band receive-only with the Global Positioning Satellite System (GPSS) using multiple fixed and tracking antennas as illustrated in Figure 2.

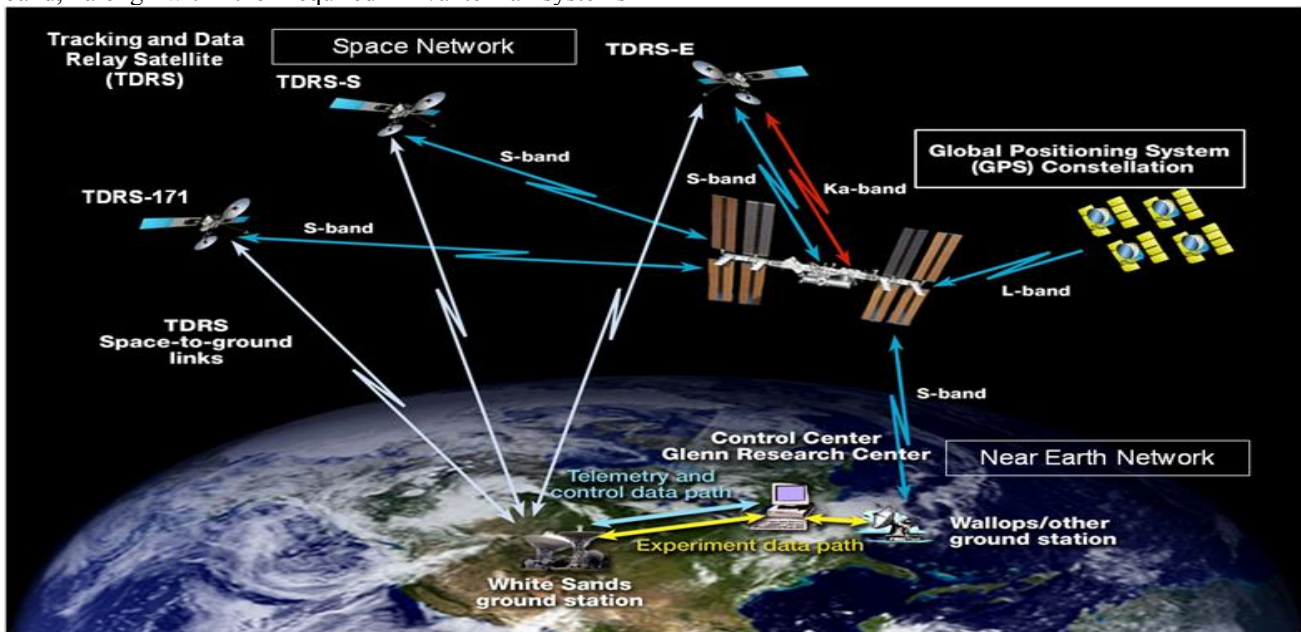


Figure 1. CoNeCT System Overview

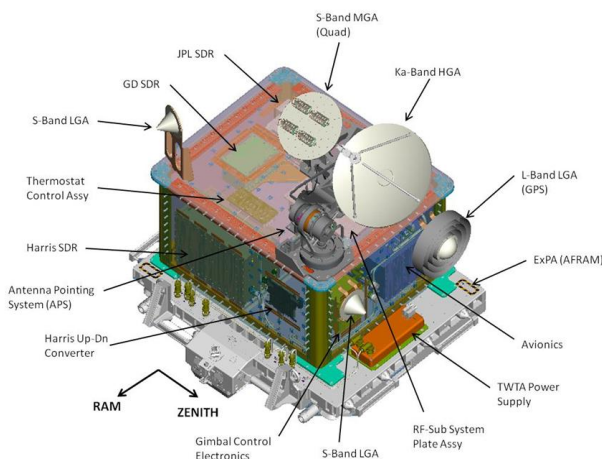


Figure 2. SCAN Testbed Major Components viewed from Ram/Zenith angle (stowed position shown)

At the core of the Flight System are three unique software defined radios provided by government and industry

partners. Each of the three software defined radios has an Operating Environment (OE), which includes an operating system and infrastructure services to applications and waveforms in accordance with the Space Telecommunications Radio System Standard (STRS). The OE middleware (compliant with the STRS Architecture Standard [1]) abstracts the SDR hardware from the waveform application software. In addition to the OE, each SDR runs waveform applications, also compliant to STRS, which implement the unique capabilities of the radio to receive and transmit radio frequency (RF) signals.

The software in the radios includes not only the code running on the General Purpose Processors (GPP) but also the logic loaded into the reconfigurable Field Programmable Gate Arrays (FPGAs). The OE includes components in both, as do waveform applications. The GPP code is primarily in C and C++. FPGA configurations are defined with Verilog and VHDL (Very high speed integrated circuit Hardware Description Language). All three SDRs use SpaceWire [2] for their data connection to the Avionics

Processor.

Procurement of the CoNNeCT SDRs

The Harris and GD SDRs were developed under a competitively competed cooperative agreement, where Harris and GD funded a significant portion of the development costs. This approach is ideal for technology development efforts such as CoNNeCT where the developer shares the risk of the new development, while benefiting from NASA's investment. A cooperative agreement provides industry an opportunity to raise the TRL of a new space product and gain valuable flight experience to fully test this new development in a space environment. NASA benefits from the opportunity to assess new concepts and technologies of interest to NASA missions such as reconfigurable SDR technology, and STRS standards development.

A cooperative agreement poses a challenge when used for flight hardware since the consequences of a late delivery or cost impact are shared among both the developer and NASA. This shifts a portion of the development risk to NASA in exchange for the cost sharing from the developer. In the end, the cooperative agreement was very successful for the Harris and GD SDRs. The delivery of the SDR units, and documentation deliverables were achieved through close technical oversight by NASA, a strong commitment by Harris and GD to deliver on schedule, and a close and open working relationship to share status, disclose problems, discuss solutions, and take actions to mitigate risk throughout development.

The JPL SDR was procured using an existing development task contract between NASA and JPL.

Common Development Approach Discussion

The focus of this paper is the unique challenges of developing and testing reconfigurable platforms for space. Many aspects of the development and test of the CoNNeCT SDRs follow typical radio hardware development processes. All SDRs underwent subsystem testing at the vendor, where platform and waveform requirements were verified and environmental tests such as thermal vacuum, vibration, and EMI were performed across the range of the specified values. Once the unit was delivered to Glenn Research Center, and at each subsequent integration point, the unit was tested for basic functionality, exercising various platform requirements and waveform requirements to ensure nothing changed or degraded as it processed through the integration steps. Once integrated into the system, and along with the RF subsystem (e.g. TWTA, coax cables, isolator, diplexer) the integrated system was tested to verify system level requirements. In addition, several characterization tests were conducted to assess performance of the radio pre-flight as a basis for the experiments planned to advance the SDR and assess performance on-orbit. Verification and characterization tests included output

signal characteristics including power, and spectral performance, frequency stability, bandwidth characterization, and on the receive side tests measured tracking and acquisition thresholds, BER performance, and others. Many of the end-to-end link tests were repeated throughout the system thermal vacuum test and EMI to understand performance over temperature and in the presence of other signals.

Documentation delivered with each radio platform (and required by the STRS Architecture) include a Hardware Interface Description (HID) document, an Interface Control Document, and an FPGA waveform application Wrapper's Guide to aid future waveform developers to develop new waveforms and facilitate the port to the SDR. The HID document provides a description of the hardware resources available to a waveform developer. The FPGA Module wrapper provides template files for future FPGA designs and provides sample interfaces. The sample interfaces are intended to abstract hide the SpaceWire and internal bus protocols. Also included are standard naming conventions for connecting to the FPGA and prototype files to aid simulation of the FPGAs

Harris Corporation Software Defined Radio

The Harris radio, shown in Figure 3, utilizes the TDRSS Ka-band forward and return service. The Harris SDR contains four Xilinx Virtex-IV FPGAs, a 1 GFLOP floating point Digital Signal Processor (DSP), an AITech 950 single board computer utilizing the VxWorks Operating System, and an S-band to Ka-band RF converter. The Harris radio is unique among the three in that it uses a second SpaceWire link for control and interface to the flight avionics. The STRS OE supplied with the Harris radio uses the Vx Works RTOS.



Figure 3. Harris SDR Picture

General Dynamics (GD) Software Defined Radio

The GD radio, shown in Figure 4, utilizes S-band for forward and return links to TDRSS or direct links to and from a ground station. The GD SDR contains an Actel RTAX, one 3 million gate Xilinx QPRO Virtex II Field Programmable Gate Array (FPGA), a ColdFire micro processor, and RF conversion module, and power amplifier. The radio transmit output power is approximately 8 Watts.

The operating system is the VxWorks Real Time Operating System (RTOS). The GD radio is controlled by the flight computer avionics via a MIL-STD-1553B link based on their heritage design.



Figure 4. GD SDR Picture

Jet Propulsion Laboratory (JPL) Software Defined Radio

The JPL radio, shown in Figure 5, utilizes S-band for forward and return links to TDRSS or direct links to and from a ground station. The JPL SDR also receives GPS frequencies of L1 (1575.42 MHz), L2 (1227.60 MHz), and L5 (1176.45 MHz). The JPL SDR contains Actel RTAX 2000 and two 3 million gate Virtex II Xilinx FPGAs, an Actel AT697 with SPARC V8 processor, RF converter section, and a power amplifier. The radio transmits a minimum of 7.5 Watts at 2287 MHz. The control interface for the JPL radio is via MIL-STD-1553B.

The STRS OE supplied with the JPL radio uses the open source RTEMS [3] RTOS. POSIX style device drivers provide the abstracted interface to GPP software of the hardware devices, including those instantiated within the Xilinx FPGAs. The OE implements a command handler and basic engineering telemetry and manages the 1553 interface.

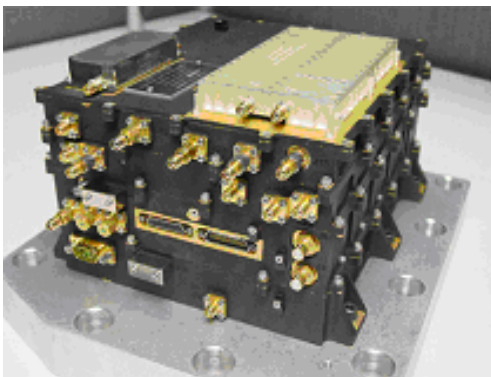


Figure 5. JPL SDR Picture

3. HARRIS SDR

Requirement's Approach

The Ka-band SDR transceiver was the first for NASA, and a well defined and tested requirements document did not

exist. The requirement development process for the Harris Ka-band SDR involved scaling the S-band TDRSS Generation IV transponder requirements, looking at other Ka-band missions (although missions were transmit only), compliance to operate within the Space Network (i.e. TDRSS), and in-house analysis. Like the other SDRs, the requirements were divided among platform requirements and waveform requirements. The goal was to define the platform separate from the waveform, so that the platform capabilities could be described independently of the waveform for future waveform developers. Based on the platform and waveform requirements and the STRS Standard provided to the developer, a single specification document was created and tracked for compliance.

There were a number of key requirements for the Harris SDR. For the platform, key requirements included operation at Ka-band frequency, compliance with the STRS architecture by providing an operating environment to abstract the application and control software running on the single board computer, have fully reconfigurable signal processing, provide an FPGA abstraction layer to enable accepting new waveforms, provide data transfer through a standard interface (Spacewire), and mitigate single event upsets and immune to single event latchups for operation in the space environment. Other platform requirements included on the RF section of the radio included a 225 MHz bandwidth for operation with TDRSS, and sufficient output power to drive the TWTA.

A key goal of the project (and subsequent requirement) was transmitting 100 Mbps from the radio over the Space Network. While the RF implementation of this requirement fell to the RF subsystem, the radio provided the waveform. The available modulations for the planned 225 MHz bandwidth service were QPSK and Staggered QPSK [5]. Requirements were then specified to operate the waveform application using SQPSK to minimize spectral regrowth from the TWTA at 100 Mbps uncoded and 100 Mbps coded using rate 1/2, constraint length 7 convolutional encoding. The resultant bandwidth of the 100 Mbps, rate 1/2 coded would be approximately 200 MHz, thus using a significant portion of the allocated 225 MHz TDRSS bandwidth.

Design and Development Approach

While the integrated SDR was a new development for Harris Corporation, the development leveraged a history of flight processor and RF systems developments. The SDR consisted of a AITech 950 single board computer, in-house designed modem board, digital IO board, ADC/DAC sampling board, transmit RF, receive RF, master reference oscillator board, and two power boards; one for modem and RF power and one to provide power to the single board computer. The boards were interconnected through a 6U compact CPI backplane. The radio assembly output was at S-band MHz and used an external RF converter to

upconvert and downconvert to the Ka-band. The integrated system with the current waveform operates at transmit center frequency of 26.560 GHz and receive center frequency of 22.6795 GHz. The platform is capable of transmitting within a frequency range of 25.25-27.5 GHz and a receive frequency range of 22.55 - 23.55 GHz

The single board computer provides the overall control and monitoring of the SDR. The board is conduction cooled, 3U cPCI size, radiation tolerant, Power PC 750 class processor, and commercial circuit board. The unit has 128 MB SDRAM, 1MB boot and 64 MB flash memory. The single board computer runs the VxWorks operating system. The single board computer loads programs from its memory into the processor and executes the programs. It also stores application bitstreams and loads them to the modem card when commanded. The computer board implements the clock function and maintains synchronization with the avionics host computer.

The digital input/output (I/O) card provides the primary mechanism for communication for the avionics processor (host computer) to the single board computer processor card and the modem card. The digital IO card uses a Spacewire interface to receive commands from the host avionics computer and deliver the commands to the processor board. The processor board also returns telemetry when commanded, averaging once per second telemetry returns. The IO card exchanges data between the host avionics and the modem card. The processor card uses the I/O card to communicate with the modem through a PCI to SpaceWire mechanism operating with the Remote Memory Addressing Protocol (RMAP) configuration. The I/O card also provides discrete signals to enable power and provide a reset function for the modem card and RF subsystems.

The modem board is a custom circuit board developed by Harris Corporation and is the core of the reconfigurable SDR. It provides the main signal processing hardware for the radio. The modem card consists of a controller ASIC, four Xilinx IV radiation tolerant FPGAs, a user programmable digital signal processor, and 256 Mbytes SDRAM with error detection and correction. The FPGAs can each accommodate one different bit stream. There are two FPGA wired to the transmit section of the radio and two FPGAs wired to the receive side. The controller ASIC includes the scrubbing functions and internal Spacewire router to move data throughout the modem card. Digital clock manager blocks are supported within each FPGA.

The breadboard, engineering model, and flight unit each are compliant with the Space Telecommunications Radio System (STRS) Architecture. Harris Corporation developed an STRS Operating Environment during the program, which provides an abstraction layer between the user's application software and the underlying hardware of the single board computer. The Ka-band waveform was also developed compliant with STRS.

An application waveform was developed alongside the platform. The waveform application provides a 300kbps to 100 Mbps variable rate, Staggered-QPSK (SQPSK) modulated transmit signal and a 300 kbps to 25 Mbps variable rate BPSK modulated receive signal. Selectable parameters of the waveform (on both transmit and receive) included rate $\frac{1}{2}$, constraint length 7 convolutional encoding/Viterbi decoding, NRZ L or M, randomizer, derandomizer, modulated or continuous wave transmit signal, and defined framing according to the Consultative Committee for Space Development Systems (CCSDS) Advanced Orbiting Systems (AOS) Space Link Protocol CCSDS 732.0-B-2. A key function required of the application was the ability to internally generate a PseudoRandom Bit Stream (PRBS) of $2^{23}-1$ length for transmit and detect and measure bit error rate on the receive link. These functions of generating and receiving data proved invaluable during all phases of system testing.

The documentation associated with the Ka-band Waveform included a Waveform User's Description (in the form of a presentation) and Interface Control Document to aid developers porting the Ka-band waveform to other platforms or reusing portions of the waveform in future developments.

The Harris SDR development included a breadboard, engineering model, and flight unit. It was envisioned that a breadboard, delivered early in the schedule, would be used for interface testing, particularly the development of the command and telemetry interface with the avionics. The breadboard was designed to be functionally equivalent to the flight system, but with output at the radios intermediate frequency (IF) instead of the final Ka-band frequency. This significantly saved costs and enabled early risk reduction testing and software development. The breadboard unit was used to develop avionics interface software, prototype waveform functions, and test interfaces with other radio slices such as the ADC/DAC sampling card and reference oscillator slice.

It was determined early in the development that once the flight unit was on-orbit, a high fidelity engineering model as close to the flight system as possible was essential to develop and verify new waveforms. Understanding the fidelity needed in the ground unit engineering model to verify future waveforms later became a primary objective of the project. Due to the aggressive schedule, the engineering model was developed along with the flight unit. Although the general approach and the author's recommendation is to develop the engineering model first, then the flight unit, developing the two units in parallel enabled many of the parts to be similar grade, but differing in screening to reduce costs. However, some of the more expensive parts used commercial equivalents. In particular for the Harris SDR, the engineering model FPGA uses a ball grid array style packaging while the flight unit uses the column grid array (CGA) packaging. The same is true for the digital signaling processor on the modem card. Memory and regulator

circuits use commercial grade parts on the engineering model compared to a higher grade space part for the flight units. Finally, there is a difference with the flight unit conformal coating and staking fasteners compared to the engineering model not using conformal coating or staking connections. The breadboard was delivered to the project in September 2009, the EM was delivered in March 2010, just ahead of the flight unit.

One aspect of the Harris SDR that differed from the other SDRs was the custom interface to test the SDR (breadboard, engineering model or flight unit). Since all three units had the same interface a common avionics simulator was developed to operate and test each unit throughout development. A sample of the interface graphical user interface shown in Figure 6 illustrates several items. First, the Ka-band waveform application properties are shown in the figure. The properties are returned in telemetry and downlinked with other flight system telemetry. Second, various functions about the transmitter and receivers functions are shown, such as CW Sig Gen Test (lit green indicates the unit is transmitting a CW signal), Tx Rtn Link FEC, and lastly Rx RF Synth Lock (lit green indicated the receive synthesizer is locked).

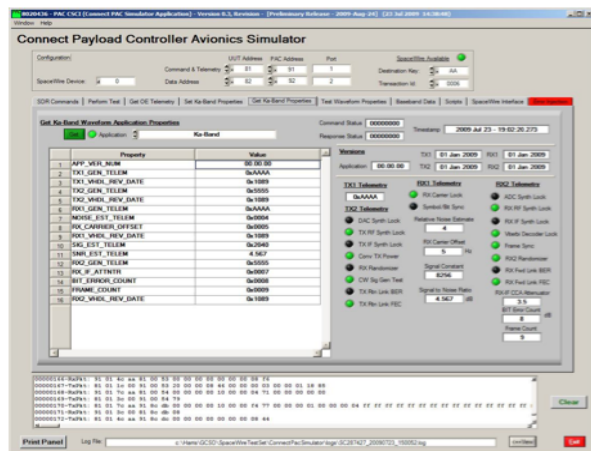


Figure 6. Avionics Simulator for the Harris SDR

Other information displayed by the simulator and later the ground software telemetry include bit error count, frame count, and receives signal to noise ratio, among others. The comprehensive test interface provide very valuable during all phases of development and testing and helped isolate problems to either the radio or control avionics.

The Ka-band SDR developed by Harris was initiated in December 2008 and the SDR was delivered in August 2010. Within these 20 months, Harris delivered the breadboard, engineering unit and flight system. The SDR development was driven mainly by schedule, followed closely by costs. Decisions about part quality on the engineering unit compared to flight often centered on costs difference, versus delivery schedule. In many instances buying a larger quantity of a flight part to use on the engineering model ended up saving time for a modest cost increase. This saved

the time of having differences in the platform and/or waveform design to accommodate the different parts. Size, mass and power were other variables traded for schedule. There was little attempt to shrink the size or power consumption of the unit as the project's mass and power budget were sufficient without spending time to optimize the design. There were a number of concepts discussed to reduce power and/or size, but not implemented due to time.

Lessons Learned

Systems Engineering - The system engineer must define and verify capabilities of the SDR while balancing specific requirements for the particular mission. Capabilities of the SDR will often exceed the minimum mission requirements, and if the additional capability is ever called into service during the mission (often unexpectedly, due to unforeseen failure or system degradation), there must be an understanding of those capabilities. Early in the requirements development, special effort was made to specify requirements associated with reconfigurability, compliance with STRS (to facilitate future waveform development), and accommodating future waveforms. Although the schedule was heavily constrained, if time permitted, additional platform characterization requirements might have included characterization of the RF bandwidth and frequency capability, beyond the intended band of operation. This would have paved the way for dynamic spectrum access experiments. While these types of experiments are still possible, they lack the preflight data across the entire bandwidth. Additional characterizations include time measurements throughout the platform to accommodate future application developments.

Since the project was driven by schedule, requirements ended up concentrating on the application waveform and links to TDRSS, in particular waveform compatibility with the Space Network. These requirements then drove verification testing leaving little time to characterize more aspects of the SDR itself. If more time were available during development, other tests would have been included such as receiver gain and noise figure control, output power response, thermal calibration, and any timing information possibly required in the future.

Development - There were a number of challenges to develop the Harris SDR on such an aggressive schedule. Many trades were made to improve performance, reduce size or power, etc. compared to the time to deliver on schedule. A situation regularly discussed was whether to repair problems known to be in software during development or defer to after delivery or even defer to on-orbit. The focus of the discussion was if the problem resided in hardware or software and what risk remained after verifying the functionality of the hardware, provided the software could be improved later. The project was centered on the ability and capability to upload new software to the flight system while on-orbit. This mission

objective shaped many decisions for not only the Harris SDR but the system in general, and many decisions were made to continue the development path of the hardware, even if the software required updates down the road. This was often the only choice to remain on schedule.

Software challenges included performance degradation in bit error rate at high E_b/N_0 on the receive signal causing the BER curve to “flare” and after a year of operation, the radio experienced random reboots. These have been resolved but are indicative of the evolving Avionics interface, which, in its final form, exposed a latent defect.

Test- For all laboratory waveform application tests and verifications, the flight system was connected to a commercial modem and signal conversion system that simulated the link between the flight system and the Space Network modem at the White Sands ground facility. The simulator’s capability included all the programmable functions within the radio including encoding/decoding, data formatting, randomization, framing, and allowed BER measurements in both the transmit and receive directions using a PRBS sequence or bit error rate measurements, respectively.

The full system test of the flight system also included a significant part of the ground system. As part of any mission using the Space Network, a special test was conducted to assess the flight system compatibility with the on-orbit TDRSS network. This test uses the flight system connected to an uplink/downlink ground station (locally near the flight system facility) which communicates directly with a TDRS which routes the signal to a space to ground link terminal at White Sands. Data from the White Sand ground terminal is routed back to the CoNNeCT Control Center using NASA’s Integrated Services Network (NISN), where the data originates or terminates to measure overall system performance. The modem at WSC modulates/demodulates and encodes/decodes as required for a particular test. Other data formatting is conducted at the experiment equipment at the Control Center.

4. GENERAL DYNAMICS SDR

The GD SDR was selected as an industry S-Band reconfigurable transceiver for space use. General Dynamics Advanced Information System (AIS) was selected as the vendor for this effort. The GD SDR represents a SDR developed by industry with a strong legacy for the space command and telemetry market where the provider develops the SDR platform, the STRS software, and the STRS compliant waveform, and provides an integrated, tested radio. This team had experience working with NASA developing the STRS architecture.

Requirement Writing Approach

The requirements were generated for the SDR platform and the S-band waveform based upon previous generations of S-band transponders. There were a number of legacy S-band

radio specifications available to start the requirements compatible with existing NASA Space Network services. The SDR requirements addressed TDRSS operations, radio specifics, and waveform/modem operation. New requirements were generated to address upgrades for new NASA services, and STRS architecture compliance. Specific payload and environmental requirements were developed for operating on ISS in a LEO environment.

New requirements were generated to address the reconfigurable nature of a SDR. One of the key challenges was developing separate requirements for the hardware platform and the waveform. A requirement was to make the operating environment and the waveform reconfigurable. OE reconfigurability allows the radio platform to support updates for new STRS architecture infrastructure capabilities, services, and operating system abstraction. The ability to change waveforms allows the radio unit to use new waveforms not present in the radio before launch. Radios may receive waveforms by the command channel or through an active waveform operating on the radio, during the waveform upload process. The new waveform can then be implemented upon the next boot or startup, or appropriate external command.

Additional requirements were generated to support safe operation and provide status of the SDR to researchers. A requirement was added to have the SDR autonomously recover from fault conditions to a known safe state after reboot or power cycle. The recovery state is defined by a system configuration file. This requirement provides ability to program certain functionality into non-programmable memory that would allow recovery to this “safe state” should an anomaly occur. The radio was required to provide a Built-In-Test (BIT) and status of the radio functionality, and last known configuration when interrogated remotely. This provides a means to access data that can be used to identify faults, and provides valuable configuration information. These capabilities improve reliability and availability by increasing the understanding of the nature of a problem leading to a faster recovery, as well as supplying additional information to assist in improving future designs and procedures. The radio is also required to detect extended loss of operation either due to signal degradation or due to internal malfunction. This capability also increases reliability and availability by allowing faster detection of a problem leading to a quicker recovery.

A technique that helped with requirement development for all three SDRs was adding rationale with the requirements. This allowed the designers to understand the intent in more detail than the traditional requirements language would allow. This also provides insight for future users of these requirements for reconfigurable SDRs, and helps develop a better verification plan.

General Dynamics used the requirements to develop detailed specifications for the manufacture of the platform and development of software. These specifications were

separated into platform and waveform specifications. The platform specifications covered details of the interfaces, hardware performance specifications, and built-in functions. The platform provides all of the baseline functionality needed to implement a TDRSS compatible transponder, including S-band up- and downconverters, an eight watt power amplifier, power converters, and a programmable digital processor module for hosting mission specific waveforms. The waveform requirements established the design and performance requirements for the TDRSS waveform. The details of the reprogrammable capabilities are contained separately in the Hardware Interface Definition document, and the software operating environment requirements are contained in the Software Requirements Specification.

Procurement Approach and Schedule

The cooperative agreement was awarded through a NASA Research Announcement (NRA), and the cooperative agreement was finalized in April 2008. The cooperative agreement was structured with a series of milestones. A series of reviews were held after each milestone, including requirements, preliminary and critical design, and acceptance.

A breadboard was delivered to GRC in February 2009. This limited capability breadboard provides a subset of CoNNeCT functionality to test the command and telemetry interface between the avionics and the SDR. The Engineering Model was delivered in April 2010 and the Flight Unit was delivered in May 2010. An additional breadboard was loaned to GRC after the design of the Digital Processing Module (DPM) for the EM and FM SDRs was finalized. The Engineering Model has similar components and fidelity as the flight system.

The low fidelity breadboard was delivered early in the project to test out the avionics command and telemetry interface. One lesson learned was that it served this purpose adequately, but is of limited use as a platform for future waveform development since it does not have the same memory and functionality as the flight DPM. The delivery of an identical DPM with the same FPGA as the flight system is recommended. This type of breadboard was intended but, due to lack of funds and schedule, only the low fidelity breadboard was delivered. This avionics interface testing helped reduce schedule and technical risk.

Since the SCAN testbed will serve as a reconfigurable testbed, having high fidelity ground models to develop and test the new software and firmware is essential for proper testing before on-orbit operation. The EM and FM have nearly identical components; the major difference was a lack of power amplifier on the EM SDR. A notable lesson was the ability to have the reprogrammable components identical to the flight unit, including the correct version of the flight components so that the testing of the timing is identical. This proved valuable and reduced the cost during development and testing.

Development Approach

GD provided an integrated platform with the STRS operating environment and TDRSS waveforms. GD has been the vendor for previous versions of the TDRSS command and telemetry transponders for NASA. The legacy radio was optimized to be highly reliable, and was optimized so that the size, weight, and power were minimized so as not to burden future resource limited space platforms.

GD leveraged the previous legacy radio design by reusing slices and components such as the RF conversion, power supplies, and the S-band Power amplifier, with minimal changes. For the CoNNeCT SDR, a reconfigurable processor, the Digital Processor Module (DPM) is new. The DPM was designed to fit within the existing form factor for the other modules.

The platform allows reprogrammability within the S-band frequencies. The transmit frequency is tunable from 2200 MHz to 2300 MHz, and the transmit frequency tuning settability is 125 kHz. The -3 dB bandwidth of the transmitter after the modulator is 6 MHz. The receive frequency is tunable from 2025 MHz to 2120 MHz. The receiver frequency tuning settability is 1 kHz.

The interfaces for the radio include a MIL-STD-1553B interface for commands and telemetry between the radio and Avionics. The data interface uses SpaceWire protocol, for forward link data provided to Avionics, and return link data received from Avionics. The unit is powered with 28 V Primary Power. There are separate power interfaces for RX Power Converter and PA Power Converter. Discrete signals are sent through a separate LVDS interface.

The key step to the GD SDR hardware development was the design and fabrication of the DPM. This design used a radiation hardened Coldfire general purpose processor with flight heritage, but added a reconfigurable Xilinx FPGA to execute waveform firmware. The development approach was to build and test a prototype of this module. Once the prototype testing was completed, some revisions were incorporated and engineering and flight modules were fabricated. One key difference between the breadboard and the EM/FM DPM is that a Actel one time programmable FPGA replaced the reprogrammable Xilinx FPGA so that waveform control functions were in a more radiation hardened package.

One unique item added to the platform was the use of a new memory device as an experimental objective. A Chalcogenide Random Access Memory (CRAM) from BAE was based on the success of the 64kb CRAM program. The CoNNeCT SDR has a 4Mb CRAM that is designed and fabricated in 0.25 μm radiation hardened CMOS. [5], [6]. The CRAM vendor provided samples of this memory in exchange for providing details of the testing from the space qualification and flight operation.

The software for the GD SDR includes boot code or start up ROM stored in PROM (SUROM), the STRS Operating Environment (OE), and waveform software and firmware.

The Start-Up Read Only Memory (SUROM) on the DPM provides capability, and hardware initialization. The SUROM is executed on Power-On Reset or by command. The SUROM boots the SDR, performs built in test (BIT) on all memory, and copies the EEPROM image into execution RAM. The SUROM initialized the hardware interfaces and validates CPU resources (SDRAM, PROM, and non-volatile memory (EEPROM)). The SUROM then copies the STRS OE from EEPROM to SDRAM, and after successful validation, control of hardware is transitioned to OE. However, if any of the validations fail, control remains with SUROM to await further instructions. The SUROM provides a state (SUROM Idle) by which avionics controller can upload new memory (OE and waveform) images and store them into EEPROM.

The STRS OE provides the interfaces and services to support waveform application execution. The OE was designed to be compliant with the STRS architecture, but minimized the overhead for processing. Developing a lightweight STRS OE was a goal to make the architecture successful for space applications. Discussions were held with the STRS software developer on the overhead of the STRS requirement on development and reuse. The STRS overhead had minimal impact with the OE. The benefits of standardizing the exchanges and upgrades between GRC and GD to work seamlessly have far outweighed the minor CPU overhead.

The S-band TDRSS waveform provides the radio functionality and was ported from code developed from previous TDRSS transponders. The waveform code consists of both software executed on the GPP and firmware executed in the reconfigurable FPGA. The waveform was designed to modulate and transmit the TDRSS S-band return link signal TX frequencies 2216.5 MHz (Single Access) and 2287.5 MHz (Multiple Access) for Data Group 1, Modes 1 and 2. This allows data rates of 24 kbaud (low rate) and 192 kbaud (high rate). Data Group 1, Mode 3 is 1 Mbaud, and Data Group 2 1 Mbaud. The waveform will track and demodulate TDRSS forward link signal for RX frequencies of 2041.0271 MHz (SA) and 2106.4062 MHz (MA). The data rates are 18 kbaud (low data rate) and 72 kbaud (high data rate). The only issues encountered were not related to STRS, but the speed of the radiation hardened memories. This resulted in the waveform code being split and a portion executed in firmware and a portion executed in software on the general purpose processor.

Good documentation is key for any development effort, and particularly for radios that will be used for a reconfigurable testbed both on the ground and in-orbit. The cooperative agreement called out for numerous documents, but higher priority was placed on the radio hardware and software development. More thorough documentation, although

contributing to increased costs, would have been valuable to reduce time spent to understand detailed operation. Increased detail in the user's guide would have helped, particularly by adding a section on typical use that would have described the detailed sequencing required of a complex SDR.

Test Approach

The experience in developing and testing the CoNNeCT GD SDR demonstrates that new functionality always needs to be tested thoroughly. Test setups need to be sufficient to fully test this capability. Contract requirements need to be very specific in the requirements to verify the capability. Checking the interfaces out in great detail as soon as possible is critical. Documents are necessary, but can be misinterpreted. For example, the simulators used for testing the SDR Spacewire interfaces did not have complete functionality. It is expensive and time consuming to develop a full simulator for all the interfaces. However, changes were identified after the unit was shipped and an update to the Spacewire interface was required and this consumed valuable time and expense later in the program. When the units were shipped from GD to GRC, benchtop acceptance test was performed to verify that the unit survived shipment and worked properly when connected to an avionics simulator and S-band TDRSS Simulator (TSIM). These tests verified operations before the installation into the flight enclosure.

One obvious item confirmed in this process is to never assume that a function will work but to always test and verify. The GD SDR executes the waveform on a Xilinx FPGA that is susceptible to single event upsets (SEUs) due to the radiation and charged particle environment in orbit, and the scrubbing process periodically computes checksums of the Xilinx FPGA image in order to detect and repair any damaged bits. The scrubbing did not function due to a misconfiguration of the burned-in Actel FPGA (an incorrect memory offset). Any SEUs to the FPGA will go undetected and unrepaired by the scrubbing process. This was an issue that was not caught until late into the testing, when testing of the engineering model at the vendor for updating and only at this late point was the programming error found. Unfortunately, it was too late to make a change to the flight unit to restore operation. One reason it was not caught was the telemetry value was in the serial interface, which was not available during the system level testing, not in the health and status telemetry.

The need to test was reiterated numerous times throughout the entire test sequence. When additional time became available, additional testing was conducted to operate the radio in more realistic scenarios. These additional tests uncovered several small issues that resulted in making either software or firmware changes.

The major lesson learned was that operating reconfigurable systems changes the approach to conducting tests. The vendor testing met the requirements for single function

performance, rather than characterizing the operation as a reconfigurable system as part of a testbed. For example, the vendor tested to meeting a specific Bit Error Rate (BER) at a specific Eb/No, rather than having a BER curve evaluated over the full operating range. The typical NASA requirement development approach is also geared toward single function validation. Requirements in this effort targeted tests for future capability only within the allowed schedule. Reconfigurable system require characterization testing over the planned (and sometimes unplanned) limits, so not only the initial capabilities are verified, but the platform is well characterized so future upgrades will have the data to know how the flight system operates. Differences between the ground system and the flight system need to also be understood, so that future test results can be correlated

5. JPL SDR

Procurement Approach and Schedule

The JPL SDR was developed by multiple entities. This approach is one representation of potential future SDR procurements where the platform developer, waveform developer, and integrator roles may not all be performed by the same company, as is traditionally done. The platform, which consists of the hardware and Operating Environment, was procured through a NASA contract with the Jet Propulsion Laboratory (JPL). JPL designed and built the Baseband Processor Module (BPM) and the GPS receiver module (GPSM). JPL in turn contracted with L3/Cincinnati Electronics (CE) to develop the S-band RF hardware and to perform final hardware integration and box level environmental tests. JPL also provided CE with the hardware control software and firmware and a test waveform to exercise the hardware. In parallel, JPL developed the OE. The OE was integrated onto the platform after CE completed the hardware integration and test.

A TDRSS-compatible waveform was developed by the Goddard Space Flight Center and Glenn Research Center. This TDRSS waveform is referred to as the Glenn/Goddard Waveform (GGT). GRC was responsible for the final integration of the waveform with the platform and all system level testing. The shared development approach is shown in Figure 7.

A waveform that receives and processes GPS signals is being developed by JPL to be installed post launch. After integration and test in the ground integration unit, the system that contains the engineering model hardware, it will be uploaded to the flight system.

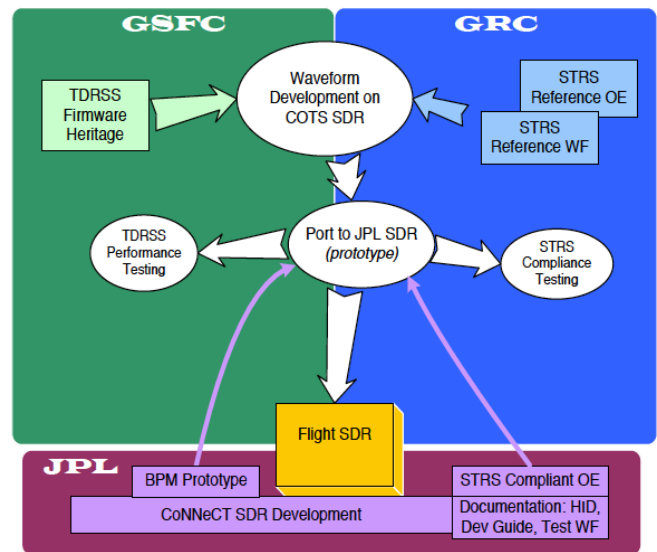


Figure 7. JPL SDR Shared Development Approach

Detailed planning and specification discussions initiated between the CoNNeCT Project in the fall of 2007. A breadboard was delivered to GRC in April 2009. The Engineering Model was delivered in March 2010 and the Flight Unit was delivered in June 2010. The Engineering Model has similar components and fidelity as the flight system. The breadboard does not contain the RF or GPS modules. JPL also purchased partial RF breadboards to verify software interfaces for the OE and a GPSM breadboard which is being used by the GPS waveform developers.

Design and Development Approach

The hardware design is based on a previous reprogrammable platform, Electra [5], which operates in the UHF frequency band with a Proximity-1 waveform. Electra was built collaboratively by JPL and Cincinnati Electronics. An existing design to upgrade the UHF components to S-band was used. The GPS slice was developed using a heritage design (Blackjack) with new parts and packaging. Requirements, development procedures, and test procedures from the Electra and Blackjack systems were tailored to develop the CoNNeCT JPL SDR.

Because of the phasing of the funding for the GPS and TDRSS waveform development, test waveforms were developed by JPL and used to test the hardware prior to the completion and integration of the TDRSS or GPS waveform. The GPS test waveform collects the samples from a test signal inserted at the L1, L2, and L5 frequencies for a short time (a few seconds). The stored file is analyzed to assess the function and performance of the GPSM.

Although the use of heritage systems was critical to completing the development in the available time, it also presented problems. Heritage products were single function devices, so the test procedures did not contain sufficient characterization.

The TDRSS waveform was also developed and integrated by multiple entities. GSFC had developed a laboratory implementation of a TDRSS waveform on a ground development system. It was not designed for the limited resources of a space platform or optimized for performance. The GSFC TDRSS development waveform included most TDRSS services along with significant debug code and enhancements for future waveforms. GRC, with assistance from GSFC, developed the CoNNeCT specific requirements, developed the documentation required for flight code and the STRS information set, converted the code to be STRS compliant, and removed extraneous code. GRC then ported the code onto the JPL flight system (following testing on the breadboard and Engineering Model), and performed the integrated test with the JPL provided OE.

The post-launch installation of the GPS waveform demonstrates the value of SDRs. Once this waveform is installed on the flight system, it will improve the capability of the testbed beyond the launch capability. The process of developing, installing, and testing a new waveform and then installing it on the flight unit will achieve one of the primary objectives of the testbed – to demonstrate the ability to upgrade the testbed after launch.

Because of time constraints, typical for any development, the Operating Environment, hardware development, and waveform development were performed in parallel. Prototypes of the system were available for the OE and waveform development. The prototype availability was crucial to the development, but documentation was being developed and revised in parallel and did not always reflect the current state of the product during the OE and waveform development phase.

Lessons Learned

The involvement of four entities in the development of the JPL SDR for CoNNeCT provided numerous opportunities for lessons learned for future multi-team developments. Due to the knowledge of all the team members in past radio development, the task was successfully completed with minor additions to the time and budget allocated and performance is satisfactory. Additional improvements to the OE and waveforms to improve performance and provide additional capabilities are proposed for future development.

System Engineering- The authors recommends that platform requirements contain additional requirements to characterize the hardware to support future waveforms. For example, a sweep for gain, slope, spurs, etc. over the entire frequency range that the hardware is capable of, not just the frequency set for the baseline TDRSS waveform frequency assignment, would provide the information needed for a future waveform that might be permitted to transmit at a different center frequency and/or bandwidth.

In a typical transponder development, the system level power and thermal constraints are decomposed and provided

to the subsystem. In the case of a software defined radio, the allocations need to be analyzed and decomposed at a much lower level. An additional challenge is the need to understand the potential power and thermal needs of future waveforms using the FPGAs. Assuming the worse case for the components may be overly conservative but obtaining measured data is not practical because this requires the implementation of a range of test waveforms.

Detailed allocation of the functions between the Operating Environment and the waveform is also needed for SDR development. For example, in the CoNNeCT JPL SDR case, a restriction was identified late in the test process about the drive level to the SSPA from the hardware manufacturer (CE) which was accepted to maintain the delivery schedule. Since the OE hadn't made a provision for this (although it is a platform infrastructure function) the TDRSS waveform implemented the code to meet the restriction. The implementation of this control was made for schedule reasons, not technical. Because this restriction control must be implemented in each waveform, the location of the control would generally be in the operating environment. Due to lack of documentation or insight, this constraint was not known in time to integrate it into the OE and therefore the TDRSS waveform, and all future waveforms, are responsible for controlling the drive level. Plans have been made to move this functionality to the OE, but awaits funding. The reprogrammability of the SDR allows fixing these situations in flight, reducing schedule impact to fix prior to shipment.

Another example where detailed interface clarification is required between the OE and waveform provider is the data interface. The SpaceWire data interface between the SDR and Avionics follows the standard, but the standard does not define the network layer and above (e.g. message lengths, formats, etc.). The CoNNeCT project requirements did not specify anything beyond the use of SpaceWire and the speed at which the link was to run, so naturally, different assumptions were made on both sides of the link.

Development- The variability between prototypes caused an issue with the receiver ADC clock and data alignment. This was not uncovered until problems with the TDRSS waveform performance were found and involvement from JPL was required to implement the correction. The problem was corrected in the FPGA wrapper, provided by the platform developer. Problems such as this will occur if the development system and final system have different components. When possible, the characterization of the differences must be accomplished and the schedule must reflect time to correct problems for differences that are uncovered during testing.

Because the OE and both waveforms (the TDRSS waveform and the GPS waveform) were required to be STRS compliant, all three teams developed using the STRS standard. The STRS standard contains abstraction requirements and documentation requirements. The OE and TDRSS teams helped develop the standard and the learning

curve to using it, and interpreting the requirements stated in the standard, was not as steep. Use of the STRS standard saved considerable development time. Using the STRS APIs and OE from the beginning limited the development needed to interface with the various hardware, such as the SpaceWire interface. There were issues uncovered in interfacing the software portions of the APIs. For example, the standard approach to commanding JPL's previous software GPS receivers uses custom binary packets. The original plan uses existing STRS configuration commands (such as "set parameter") with the "set-to" value as the pre-existing binary command. This command would be passed to existing command interpretation code internally. This plan was adjusted when the team learned that the STRS commands didn't support binary arguments, and weren't likely to near term. So the GPS team came up with another scheme, basically inventing a parallel set of commands that could be done in ASCII.

Test-The use of test waveforms to characterize the platform was crucial. The test waveform was used to test the basic hardware functionality, including thermal performance and EMI/EMC requirements. Additional uses of the test waveform by the platform manufacturer, vs. the integrator, would have been helpful. These additional tests should include component calibrations, such as the power amplifier input/output data, calibration of telemetry items, and I/Q balance. Calibration tables could then be provided by the platform developer for all future waveform developments. The requirements process did not specifically call out characterization requirements, but instead, requirements were written in terms of end-to-end performance (as for conventional radios). To save time and money, requirements for test data were inherited from previous implementations which had no characterization requirement. As a result, the work scope for characterization, calibration, and dissemination of the characterization data was seen as a schedule risk. The waveform development team did some characterization, but lack of familiarity with the underlying hardware and OE platform and interpretation of existing calibration data led to inefficiencies in this approach.

Documentation-The STRS documentation requires that the platform developer provide a Hardware Abstraction Layer (HAL) and a Hardware Interface Description. The HAL is the library of software functions in the STRS OE that provides a platform vendor specific view of the specialized hardware by abstracting the underlying physical hardware interfaces. The HAL allows integration of the specialized hardware with the General Purpose Module (GPM) so that the STRS OE can access functions implemented on the specialized hardware of the STRS platform. The HID describes the functionality, interfaces and performance of each internal platform module and the entire radio platform.

The HAL and HID provided by JPL was not mature enough to be used without further insight from JPL for development of the waveform. This was partially due to the parallel development process of the platform, OE, and waveform.

Many conversations between the two teams were required to obtain additional information and clarify contents. Tests to verify the accuracy of the HID and HAL details were not sufficient in all cases, causing additional diagnostic time spent during integration.

The content of the required documentation set is another area of study. Requiring that both the platform and waveform developer provide the correct specifications without placing an undue burden for information is needed. As new waveforms are developed and the documentation set is tested, improvements will be made in the overall documentation set and better balance achieved.

6. SUMMARY AND CONCLUSION

This paper describes the approach used for the development of the three SDRs for the SCAN testbed. It describes at a high level the design of the SDR, the procurement approach, the requirement development, and the testing. Recommendations by the authors for future SDR developments are stated. Future papers containing detailed information on the lessons learned and the on-orbit operation experience are expected.

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